AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A synchronous clock supply system comprising:

at least one relay node which is positioned in a clock supply route formed by coupling arbitrary virtual paths for a loop of nodes in a network; and

a termination node which is positioned in a downstream side of the clock supply route farther than the relay node from a synchronous clock sending source used to synchronize the nodes in the network, and finally receives the synchronous clock via a predetermined port,

the relay node having

fault detection means for, when no synchronous clock is supplied in a downstream direction from an upstream side of the clock supply route due to a fault in the virtual path, detecting that no synchronous clock is supplied,

fault notification data transmission means for, when said fault detection means detects the fault, sending fault notification data representing occurrence of the fault to the downstream side of the clock supply route, and

first port switching means for, when switching instruction data designating switching to another port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route, switching a port for receiving the synchronous clock to the port, and

the termination node having

second port switching means for, when another port is connected to the sending source via another virtual path and the fault notification data is sent from the relay node, performing port switching for supplying the synchronous clock from the predetermined port to said another port, the first and second port switching means forming upstream and downstream switching ports, and

port switching instruction means for, when said port switching means performs port switching, sending switching instruction data which instructs the upstream side of the clock supply route to switch the port to said another port for supply of the synchronous clock.

2. (original) A system according to claim 1, further comprising clock sending means for sending the synchronous clock to the clock supply route.

3. (original) A system according to claim 1, wherein

the clock supply route includes a plurality of clock supply routes,

the synchronous clock is sent to the respective clock supply routes,

the relay node includes relay nodes for the respective clock supply routes, and

the termination node includes termination nodes for the respective clock supply routes.

4. (original) A system according to claim 1, wherein

the synchronous clock includes a synchronous clock which is obtained by extracting a frequency component from a signal used for communication between the nodes and has a unit time as a period,

said fault notification data transmission means sends the fault notification data as part of an ATM cell,

when the switching instruction data is sent as part of an ATM cell from the upstream direction, said first port switching means switches the port for receiving the synchronous clock to a port which receives the switching instruction data,

when the fault notification data is sent as part of the ATM cell from the relay node, said second port switching means switches the port for supplying the synchronous clock from the predetermined port to said another port, and

said port switching instruction means sends the switching instruction data as part of an ATM cell.

5. (original) A system according to claim 4, wherein

the clock supply route includes a plurality of clock supply routes,

the synchronous clock is sent to the respective clock supply routes,

the relay node includes relay nodes for the respective clock supply routes, and

the termination node includes termination nodes for the respective clock supply routes.

6. (original) A system according to claim 1, wherein

a priority is set for a port to be switched, and

a clock supply line priority table representing a priority for port switching for supplying the synchronous clock is prepared at each node.

7. (currently amended) A synchronous clock supply method comprising the steps of:

sending a synchronous clock used to synchronize nodes in a network from a synchronous clock sending source to a termination node along a predetermined clock supply route via a plurality of nodes;

when the synchronous clock sent in the synchronous clock sending step generates a fault in a line after the synchronous clock sending source, detecting the fault at a predetermined port at a nearest downstream node in the fault generated line;

sending fault notification data representing occurrence of the fault from the detecting node in the fault detection step to the termination node;

when the fault notification data sent in the fault notification data sending step reaches the termination node, switching a port for receiving the synchronous clock to a port which is connected to a path other than the synchronous clock sending source and the clock supply route and is different from the port that has received the fault notification data at the termination node, and sending back switching instruction data representing port switching ~~through the clock supply route~~ by coupling arbitrary virtual paths for nodes; and

switching the receiving port to a synchronous clock reception port at each node which has received the switching instruction data sent in the port switching instruction step.

8. (canceled)

9. (original) A method according to claim 8, wherein

in the synchronous clock sending step, a frequency component is extracted from a signal used for communication between the nodes in order to synchronize the nodes in the network, and is used as a synchronous clock having a unit time as a period,

in the fault notification data sending step, the fault notification data is sent as part of an ATM cell, and

in the port switching instruction step, the switching instruction data is sent as part of an ATM cell.

10. (new) A system according to claim 1, wherein there are four nodes.

11. (new) A method according to claim 7, wherein there are four nodes.

12. (new) A system according to claim 1, wherein at least one node is a switching unit comprising:

a control unit;

a clock supply line priority table connected to the control unit;

a linearly arranged input line unit ATM switch and output line unit, each connected to the control unit;

a line master unit connected to the control unit;

a linearly connected clock generation source and clock input circuit connected to the line master unit; and

at least one clock input circuit connected to the line master unit.

13. (new) A method according to claim 13, wherein at least one node is a switching unit comprising:

a control unit;

a clock supply line priority table connected to the control unit;

a linearly arranged input line unit ATM switch and output line unit, each connected to the control unit;

a line master unit connected to the control unit;

a linearly connected clock generation source and clock input circuit connected to the line master unit; and

at least one clock input circuit connected to the line master unit.

14. (new) A method according to claim 7, wherein the plurality of nodes form a loop.

15. (new) A method according to claim 7, wherein the ports comprise upstream and downstream ports.

16. (new) A synchronous clock supply system comprising:

at least one relay node which is positioned in a clock supply route formed by coupling arbitrary virtual paths for a loop of nodes in a network; and

a termination node which is positioned in a downstream side of the clock supply route farther than the relay node from a synchronous clock sending source used to synchronize the nodes in the network, and finally receives the synchronous clock via a predetermined port,

the relay node having

a fault detector for, when no synchronous clock is supplied in a downstream direction from an upstream side of the clock supply route due to a fault in the virtual path, detecting that no synchronous clock is supplied,

a fault notification data transmitter for, when said fault detector detects the fault, sending fault notification data representing occurrence of the fault to the downstream side of the clock supply route, and

a first port switch for, when switching instruction data designating switching to another port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route, switching a port for receiving the synchronous clock to the port, thereby forming upstream and downstream switching ports, and

the termination node having

a second port switch for, when another port is connected to the sending source via another virtual path and the fault notification data is sent from the relay node, performing port switching for supplying the synchronous clock from the predetermined port to said another port, and

a port switching instruction device for, when said port switches perform port switching, sending switching instruction data which instructs the upstream side of the clock supply route to switch the port to said another port for supply of the synchronous clock.

17. (new) A system according to claim 16, further comprising a clock sending device for sending the synchronous clock to the clock supply route.

18. (new) A system according to claim 16, wherein

the clock supply route includes a plurality of clock supply routes,

the synchronous clock is sent to the respective clock supply routes,

the relay node includes relay nodes for the respective clock supply routes, and

the termination node includes termination nodes for the respective clock supply routes.

19. (new) A system according to claim 16, wherein there are four nodes.

20. (new) A system according to claim 16, wherein at least one node is a switching unit comprising:

a control unit;

a clock supply line priority table connected to the control unit;

a linearly arranged input line unit ATM switch and output line unit, each connected to the control unit;

a line master unit connected to the control unit;

a linearly connected clock generation source and clock input circuit connected to the line master unit; and

at least one clock input circuit connected to the line master unit.